

FIG. 1

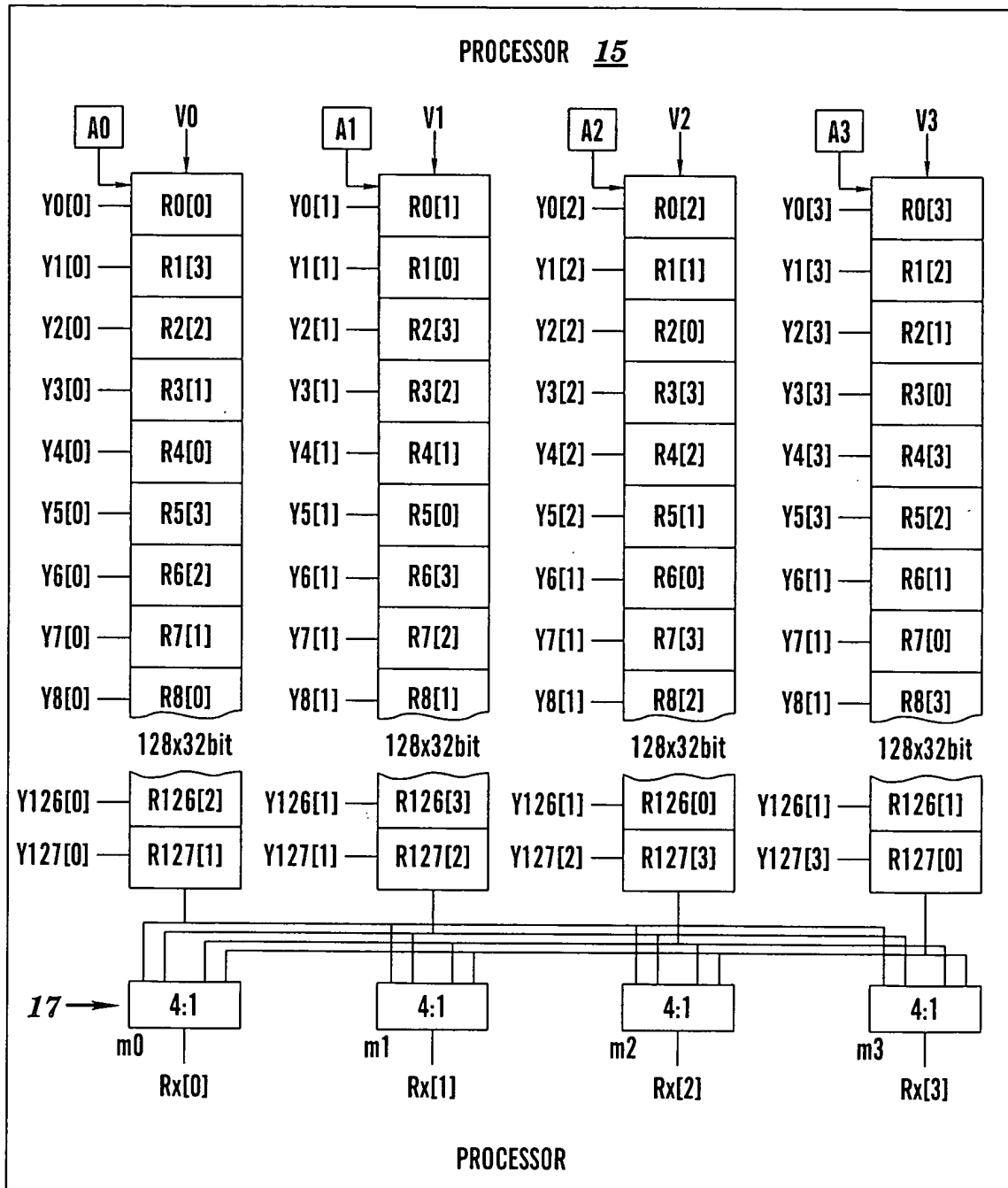


FIG. 2

20
↓

	21 ↓	22 ↓	23 ↓	24 ↓	25 ↓	26 ↓	27 ↓	28 ↓	29 ↓
REG Rx	A0	A1	A2	A3	m0	m1	m2	m3	
R0	0	0	0	0	0	1	2	3	
R1	1	1	1	1	1	2	3	0	
R2	2	2	2	2	2	3	0	1	
R3	3	3	3	3	3	0	1	2	
R4	4	4	4	4	0	1	2	3	
R5	5	5	5	5	1	2	3	0	
R6	6	6	6	6	2	3	0	1	
⋮									
R126	126	126	126	126	2	3	0	1	
R127	127	127	127	127	3	0	1	2	
R128	0	1	2	3	0	1	2	3	
R129	3	0	1	2	1	2	3	0	
R130	2	3	0	1	2	3	0	1	
R131	1	2	3	0	3	0	1	2	
R132	4	5	6	7	0	1	2	3	
R133	7	4	5	6	1	2	3	0	
⋮									
R254	126	127	124	125	2	3	0	1	
R255	125	126	127	124	3	0	1	2	

FIG. 3

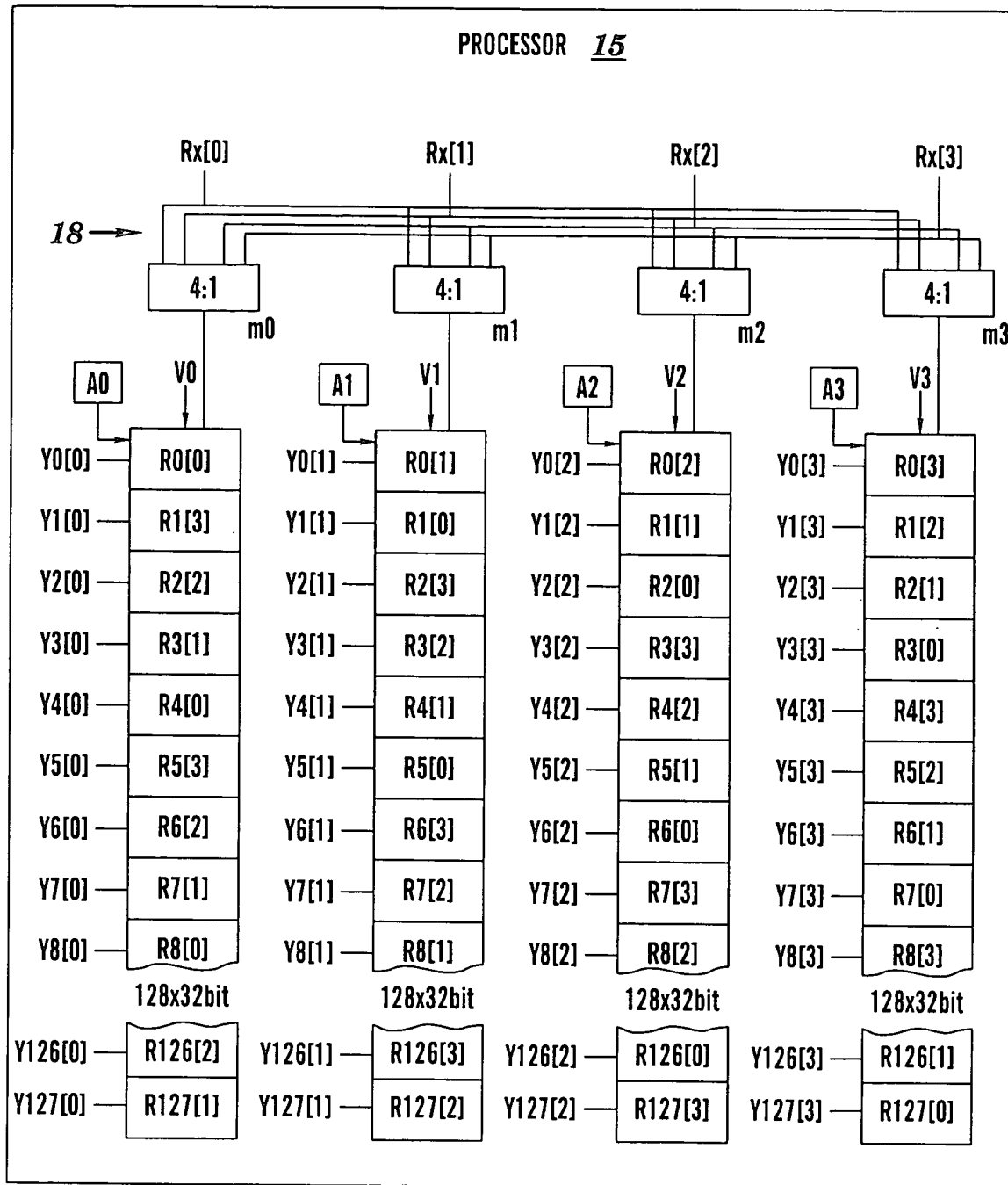


FIG. 4

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REG Rx	A0	A1	A2	A3	m0	m1	m2	m3
R0	0	0	0	0	0	1	2	3
R1	1	1	1	1	3	0	1	2
R2	2	2	2	2	2	3	0	1
R3	3	3	3	3	1	2	3	0
R4	4	4	4	4	0	1	2	3
R5	5	5	5	5	3	0	1	2
R6	6	6	6	6	2	3	0	1
⋮								
R126	126	126	126	126	2	3	0	1
R127	127	127	127	127	1	2	3	0
R128	0	1	2	3	0	1	2	3
R129	3	0	1	2	3	0	1	2
R130	2	3	0	1	2	3	0	1
R131	1	2	3	0	1	2	3	0
R132	4	5	6	7	0	1	2	3
R133	7	4	5	6	3	0	1	2
⋮								
R254	126	127	124	125	2	3	0	1
R255	125	126	127	124	1	2	3	0

FIG. 5

REGISTER MOVE/COPY WITH SOURCE SELECTION: rDEST ← rRA[aa,bb,cc,dd]

OPCODE	DEST	RA	aa	bb	cc	dd
8 BITS	8 BITS	8 BITS	2 BITS	2 BITS	2 BITS	2 BITS

FIG. 6A

REGISTER MERGE UNDER MASK: rDEST ← (rDEST, rRA)

OPCODE	DEST	RA	reserved	mask
8 BITS	8 BITS	8 BITS	4 BITS	4 BITS

FIG. 6B

SCALAR/VECTOR 3 OPERAND FP INSTRUCTION: rDEST ← f(rRB, rRA [aa,aa,aa,aa])

OPCODE	aa	DEST	RA	RB
6 BITS	2 BITS	8 BITS	8 BITS	8 BITS

FIG. 6C

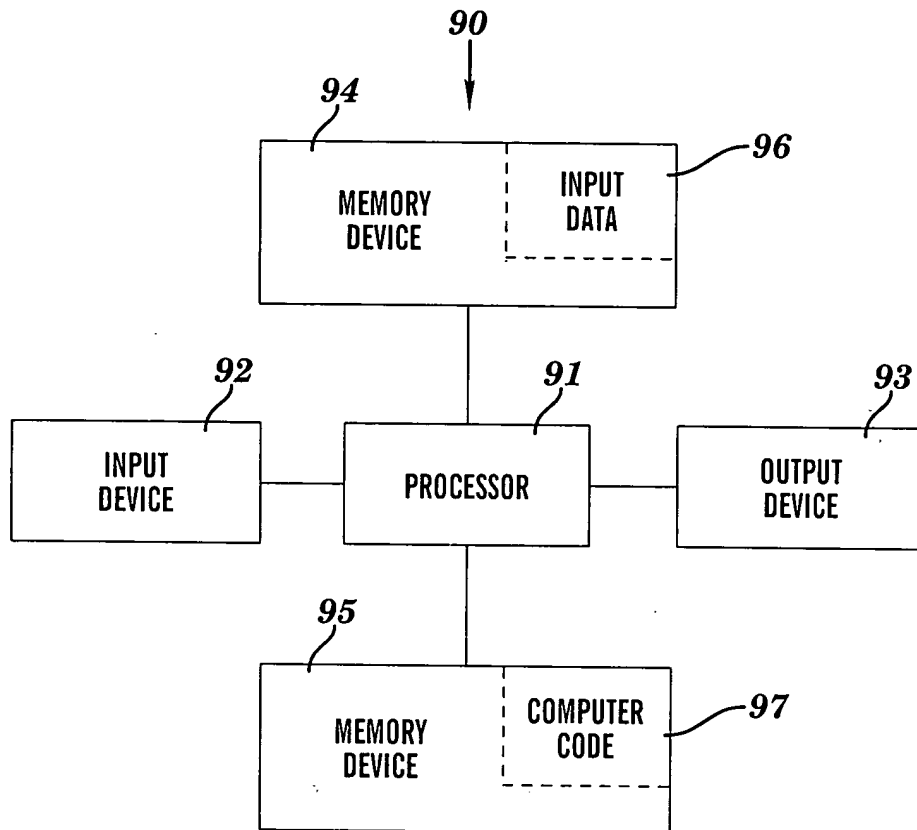


FIG. 7